emission, favorable transport properties (e.g., high electron mobility and saturation velocity), a high breakdown field, and high thermal conductivity. According to embodiments of the present invention, gallium nitride (GaN) epitaxy on pseudo-bulk GaN substrates is utilized to fabricate vertical GaN-based semiconductor devices not possible using conventional techniques. For example, conventional methods of growing GaN include using a foreign substrate such as silicon carbide (SiC). This can limit the thickness of a usable GaN layer grown on the foreign substrate due to differences in thermal expansion coefficients and lattice constant between the GaN layer and the foreign substrate. High defect densities at the interface between GaN and the foreign substrate further complicate attempts to create vertical devices, including power electronic devices such as JFETs and other field-effect transistors.

[0015] Homoepitaxial GaN layers on bulk GaN substrates, on the other hand, are utilized in the embodiments described herein to provide superior properties to conventional techniques and devices. For instance, electron mobility, μ, is higher for a given background doping level, N. This provides low resistivity, ρ, because resistivity is inversely proportional to electron mobility, as provided by equation (1):

$$\rho = \frac{1}{q\mu N}, \tag{1}$$

where q is the elementary charge.

[0016] Another superior property provided by homoepitaxial GaN layers on bulk GaN substrates is high critical electric field for avalanche breakdown. A high critical electric field allows a larger voltage to be supported over smaller length, L, than a material with a lower critical electric field. A smaller length for current to flow together with low resistivity give rise to a lower resistance, R, than other materials, since resistance can be determined by the equation:

$$R = \frac{\rho L}{A}, \tag{2}$$

where A is the cross-sectional area of the channel or current path.

[0017] In general, a tradeoff exists between the physical dimension of a device needed to support high voltage in a device's off-state and the ability to pass current through the same device with low resistance in the on-state. In many cases GaN is preferable over other materials in minimizing this tradeoff and maximizing performance. In addition, GaN layers grown on bulk GaN substrates have low defect density compared to layers grown on mismatched substrates. The low defect density will give rise to superior thermal conductivity, less trap-related effects such as dynamic on-resistance, and better reliability.

[0018] Among the vertical device structures contemplated is a vertical JFET. Depending on doping levels, physical dimensions, conductivity type (e.g., n-type or p-type materials), and other factors, vertical JFETs can be designed to have normally-off or normally-on functionality. A normally-off vertical JFET is particularly useful due to its ability to prevent current flow if no voltage is applied to the gate, which can serve as, among other things, a safety feature for vertical JFETs used in power applications.

[0019] A normally-off vertical JFET can be created in various ways. For example, an n-type current path from source to drain can be gated on either side by p+ gates. With sufficiently low background doping, and high positive charge due to high hole concentration in the p+ gates, the channel can be depleted of carriers, or pinched off at zero bias. When a positive voltage is applied to the gate(s), the channel can be re-opened to turn the device on. Thus, in embodiments of the present invention, the vertical JFET is referred to as a vertical junction field effect transistor since the current flows vertically between the source and drain through the gated region.

[0020] In addition to the ability to support high-voltage, low-resistance JFET applications, the GaN vertical JFETs described herein can differ from traditional vertical JFETs in other ways. For example, other semiconductors used to manufacture vertical JFETs, such as SiC can be utilized, altering the mode of manufacture. Furthermore, the use of GaN epitaxial layers can allow for non-uniform dopant concentrations as a function of thickness within the various layers of the vertical JFET, which can optimize the performance of the device.

[0021] FIG. **1** is a simplified cross-sectional diagram illustrating a vertical JFET **100** according to an embodiment of the present invention. Referring to FIG. **1**, a drain **101** is provided. According to the embodiment of the present invention illustrated in FIG. **1**, the substrate is an n-type GaN substrate, but the present invention is not limited to this particular material. In other embodiments, substrates with p-type doping are utilized. Additionally, although a GaN substrate is illustrated in FIG. **1**A, embodiments of the present invention are not limited to GaN substrates. Other III-V materials, in particular, III-nitride materials, are included within the scope of the present invention and can be substituted not only for the illustrated GaN substrate, but also for other GaN-based layers and structures described herein. As examples, binary III-V (e.g., III-nitride) materials, ternary III-V (e.g., III-nitride) materials such as InGaN and AlGaN, and quaternary III-V (e.g., III-nitride) materials such as AlInGaN are included within the scope of the present invention. Additionally, embodiments can use materials having an opposite conductivity type to provide devices with different functionality. For example, embodiments provided herein focus on the formation of a JFET with an n-type drain and channel regions. However, a p-type JFET can be formed by using materials with opposite conductivity (e.g., substituting p-type materials for n-type materials, and vice versa) in a similar manner as will be evident to one of skill in the art.

[0022] Coupled to the substrate comprising the drain, is a drift region **103** of n-type GaN material. The drift region **103** provides a medium through which current can flow in the device's on-state in a vertical direction from the drain to a channel region **108** coupled to the drift region **103**. In the off-state, the drift region provides a medium for supporting the electric field created by the voltage gradient between the source or gate and the drain. The channel region **108** also can comprise an n-type GaN material that is as wide as possible to minimize added resistance when the vertical JFET **100** is turned on, but narrow enough to provide adequate current pinch off when the vertical JFET **100** is turned off. The channel region **108** is coupled to a source region **106** comprising a heavily-doped n-type GaN material.